25.8 A 50GS/s Distributed T/H Amplifier in 0.18µm SiGe BiCMOS

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The increasing use of digital receivers in high-bit-rate optical transceivers and millimeter-wave radios demands increasing ADC sampling rate to support wide bandwidth and dynamic ranges required in such receivers. A broadband THA is a critical component in the high-sampling-rate ADC to overcome the limitation on the analog-signal bandwidth and account for the linearity degradation from the long settling time and nonlinear parasitic, thus reducing timing jitter. Considerable progress has been made toward the realization of monolithic THAs with the rapidly decreasing feature sizes of semiconductor technologies. SiGe-based [1, 2, 3] and InP-based [4] THAs have been recently developed with high sampling rate (> 10GS/s) and relatively low dynamic range (< 38dB). In this paper, a THA design with distributed microstrip lines to enhance the bandwidth is demonstrated using a 0.18µm SiGe BiCMOS technology. A 3-stage distributed THA (DTHA) samples an analog input signal beyond 50GS/s with an SFDR better than 40dB.

As distributed circuits operate based on multiple parallel signal paths working in synchronization, they can enhance the frequency range of operation and dynamic range [5], despite some trade-offs in ability to obtain very high gain or very low noise figure. Figure 25.8.1 shows a differential multi-stage DTHA that consists of switch stages distributed in parallel between a pair of input transmission lines and a pair of output transmission lines. The delay between the switch stages must be matched for the input and output transmission lines such that the signals add in phase. The inductive components of the transmission lines will contribute to increase the bandwidth of the switch, incorporated with the RC time-constant of the switch. The input buffer and clock buffer are also implemented with distributed topologies to enhance the input and clock signal bandwidths.

A prototype 3-stage DTHA is illustrated in Fig. 25.8.2. All building blocks are fully differential. The DTHA has a lumped input buffer consisting of an emitter-degenerated differential amplifier preceded by a pair of emitter followers. The input has 50Ω on-chip resistors to provide a good input match. The input buffer provides unity gain and very low output impedance to drive the distributed switched emitter followers and output buffer (SEFOB) stages. To avoid multiple reflections between the input buffer output and the termination of the distributed SEFOB input line, the differential amplifier has load resistors of 50Ω, which approximately match the image impedance of the distributed SEFOB stage. Active current sources are used for all building blocks to enhance the CMRR at low frequencies and provide a more flexible way to modulate the current. A relatively high bias current of 16mA is supplied to make an input buffer more linear and turn the switched emitter follower (SEF) completely off during hold mode.

The distributed SEFOB stages consist of 3 identical SEFs and output buffers connected by balanced microstrip transmission lines (Z_0 = 50Ω). To suppress the signal-dependent modulation of the base-emitter voltage of the SEF, it uses a relatively high bias current of 5.4mA. The DTHA design is focused on attaining the largest bandwidth at a maximum hold-mode performance. To reach this goal, the hold capacitors must be optimized. The hold capacitance of 200fF (170fF MIM capacitor + ~32fF parasitic capacitance) is designed to guarantee 6b of linearity. The output buffer has a pair of emitter followers followed by an emitter-degenerated differential amplifier to reduce differential droop rate. The distributed outputs are matched to 50Ω by balanced termination resistors.

The clock distribution is the most important factor to account for sampling jitter. Figure 25.8.3 shows a schematic diagram of the clock buffer. The cascode architecture is used to decrease the capacitive loading of the output and to minimize the bandwidth degradation caused by Miller capacitance. Simulations show that the bandwidth of the clock buffer is > 60GHz and the gain is 9dB. The distributed output stage generates the sequence of 'Track' and 'Hold' control signals for the SEFOB cells. Thus, the transmission-line length should be matched to those of the distributed output lines of the input buffer. The microstrip-line unit length is chosen to be 200µm in order to maximize the bandwidth. All differential microstrip transmission lines are implemented with a 2.8µm thick aluminum top metal layer (M6) that has a width of 15µm and spacing of 30µm for 50Ω, with M1 ground plane. The large spacing of 150µm is required between the input and output lines to minimize the coupling between them.

The 3-stage DTHA is designed in a 0.18µm SiGe BiCMOS. Two supply voltages are used: 4V for the THA and 3.3V for the output buffer. At the clock frequency of 50GHz, power dissipation is 640mW. The DTHA is characterized on wafer using an RF probe station. The S-parameter data is measured with an Agilent E8361A 67GHz network analyzer (Fig. 25.8.4). The forward gain (S_{21}) reaches –6.8dB (including 6dB loss from the single-ended measurement), and the reverse isolation (S_{12}) is better than 35dB. The track-mode –3dB bandwidth of the DTHA exceeds 42GHz, while simulation estimates the bandwidth of 48GHz in a differential topology. Measured DTHA input return loss (S_{11}) is <–12dB and the output reflection (S_{22}) is –9dB up to 47GHz, where there is a resonance due to the K-connectors. The 2-tone intermodulation tests are performed using the Agilent E4448A spectrum analyzer. Using 2 tones of f_1 = 30GHz and f_2 = 30.1GHz at an input power of 0dBm, the 3rd-order intermodulation distortion is measured to be about -40 dB below the fundamental, as shown in Fig. 25.8.5. The DTHA exhibited an IIP3 of +21dBm, thereby the SFDR is +42dBc with the simulated input-referred noise power of -41.5dBm. The spectral characteristic of the beat frequency test with $f_{IN} = f_S + \Delta f$, where f_S = 40 GHz and Δf = 1MHz at an input power of 0dBm, is shown in Fig. 25.8.6 with the 3rd-order harmonic distortion better than -35dB. Figure 25.8.7 shows the chip micrograph. The chip occupies a total area of 1.28×1.15mm^2, and the active area is 0.9×0.7mm^2.

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References:
[1] J.C. Jensen, L.E. Larson, "A Broadband 10-GHz Track-and-Hold in Si/SiGe HBT Technology," *IEEE J. Solid-State Circuits,* vol. 36, pp. 325-330, 2000.
[2] Y. Lu, W.M. Lance, X. Li, et al., "An 8-bit 12 GSample/s SiGe Track-and-Hold Amplifier," *BCTM Digest*, pp. 148-151, Oct., 2005.
[3] S. Shahramian, et al., "A 40-GSample/s Track & Hold Amplifier in 0.18µm SiGe BiCMOS Technology," *CSICS Digest*, pp. 101-104, Nov., 2005.
[4] J. Lee, A. Leven, J.S. Weiner, et al., "A 6-bit 12-GS/s Track-and-Hold Amplifier in InP DHBT Technology," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1533-1539, Sept., 2003.
[5] A. Hajimiri, "Distributed Integrated Circuits: An Alternative Approach to High-Frequency Design," *IEEE Communications Magazine*, pp. 168-173, Feb., 2002.

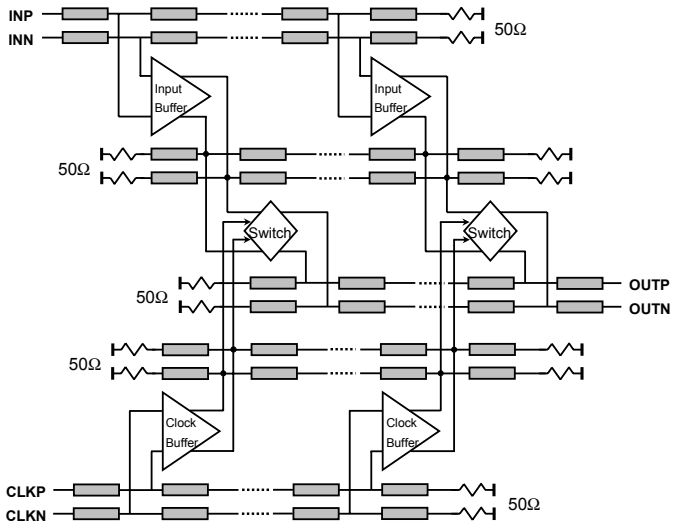

Figure 25.8.1: A schematic of differential multi-stage DTHA.

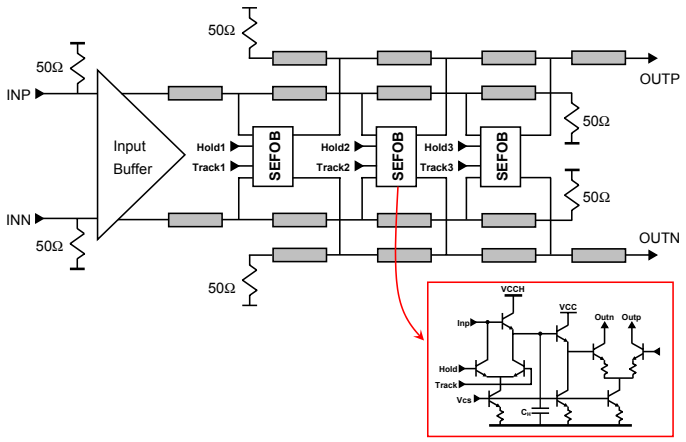

Figure 25.8.2: A schematic diagram of a 3-stage DTHA.

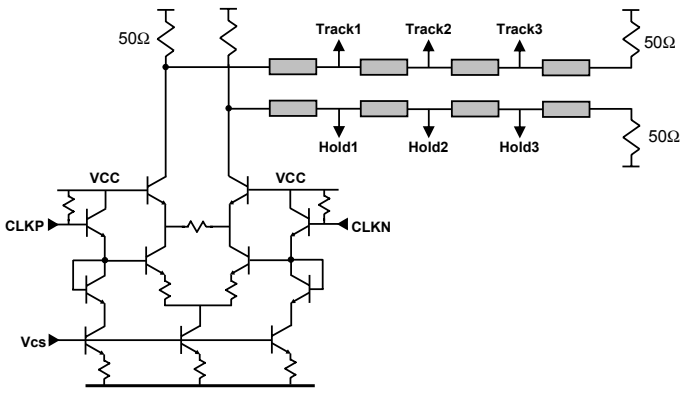

Figure 25.8.3: Schematic of the clock buffer in DTHA.

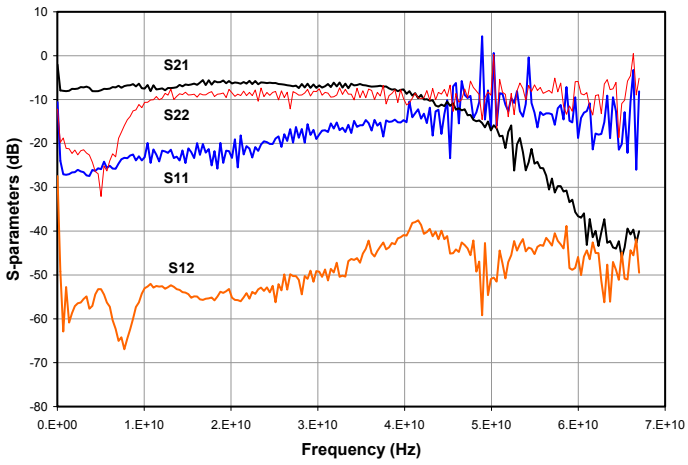

Figure 25.8.4. Measured single-ended S-parameters.

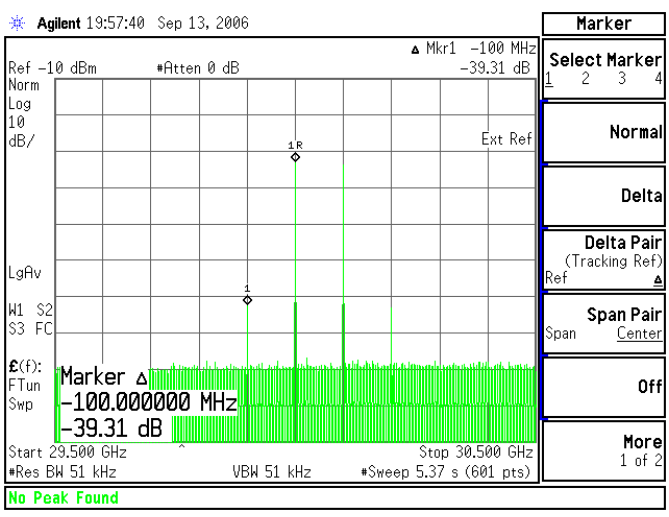

Figure 25.8.5: Measured two-tone test at 30GHz input frequency.

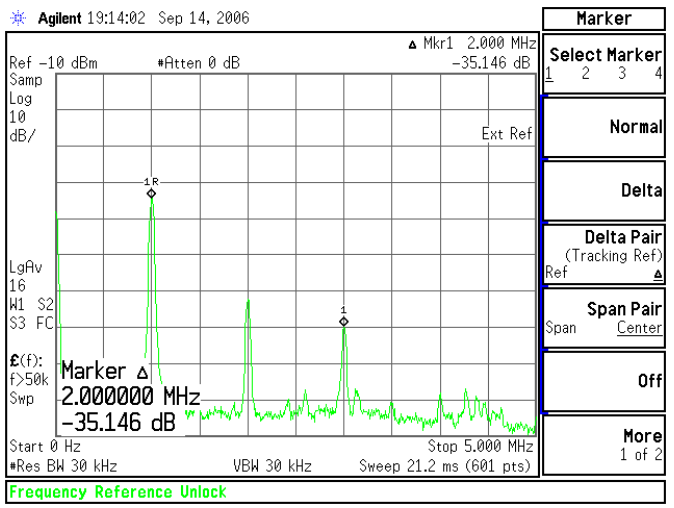

Figure 25.8.6. Beat frequency test with 40GHz input signal sampled at 39.999GS/s (single-ended measurements).

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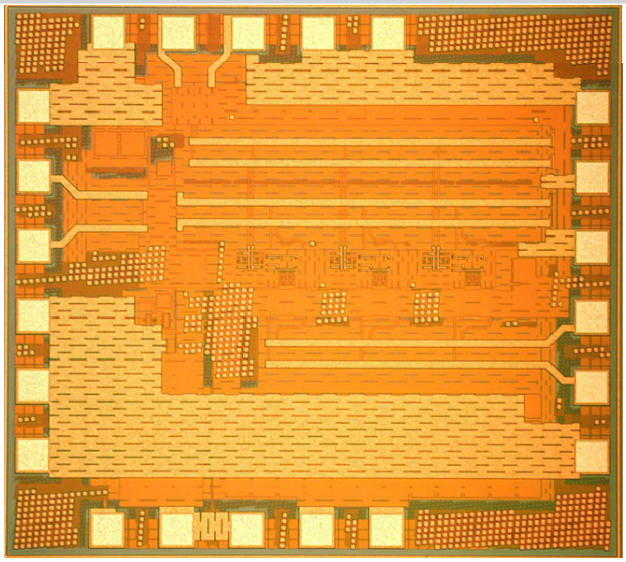

Figure 25.8.7: Die micrograph.

